



Asynchronous Techniques for Noise Tolerant Nanoelectronics

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6. AUTHOR(S) Alain J. Martin, Mika Nystroem

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Situs Logic
1442 Lomite Drive
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13. ABSTRACT (Maximum 200 words)
The objective of this Phase I study was to demonstrate the advantages of asynchronous (clockless) VLSI techniques with respect to noise tolerance, to determine the susceptibility of asynchronous QDI logic to noise-induced Single Event Upsets (SEU), and to propose solutions to detect and possibly correct SEU errors. A logical model based on production rules was developed in which the effect of an SEU is represented as the random flipping of a single bit in the boolean representation of a circuit. Contrary to common belief, the study proves that an SEU will not necessarily lead to a deadlock, and that other forms of malfunctions may result: the circuit may duplicate an output or lose an input. Modifications to the circuit implementation of production rules have been proposed such that an SEU will always lead to deadlock. Further methods have been developed to detect and correct single-bit upsets at the circuit level, with no change in system architecture, and little overhead on performance. In combination with the natural tolerance of QDI circuits to slow parameter shifts and time variations, this study suggests that it is possible to build high-performance asynchronous hardware that is tolerant to noise.

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Asynchronous Techniques for Noise Tolerant Nanoelectronics

Alain J. Martin, Mika Nyström

Situs Logic

1442, Lomita Drive

Pasadena, CA 91106

(626) 799-7830

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1. Summary

The work performed under Phase I of this contract was to study the susceptibility of asynchronous nanoscale designs to noise upset, in particular radiation or EMI, and to propose means and strategies to detect and correct the effects of noise at the electrical and system levels.

First, a logical model based on *production rules* was developed to model and analyze the effects of SEU on asynchronous devices at the logical level. The model was used to represent the effect of a SEU as the random flipping of a single bit in the boolean representation of a circuit.

The model was applied to the analysis of the behavior of the most general building-block in asynchronous technology: the so-called precharged half-buffer (PCHB). The result of the analysis shows that contrary to common belief, a single-event upset modelled as a single bit flip can bring the circuit into several illegal states: (1) the circuit may deadlock, (2) the circuit can duplicate an output, (3) the circuit can lose an input.

While it was commonly believed that an SEU will result in deadlock, behaviors (2) and (3) were not anticipated, and complicate the problem.

Secondly, modifications to the circuit implementation of production rules have been proposed such that any SEU modelled as a bit flip will always result in deadlock, eliminating behaviors (2) and (3). These techniques work in general and are not restricted to the precharged half-buffer.

Thirdly, system-level approaches to deadlock recovery have been envisioned to bring the system back into a valid recovery state.

Fourthly, methods have been proposed to detect and correct single-bit upsets at the circuit level, with no change in system architecture.

Fifthly, optimizations have been proposed that reduce the cost of SEU detection and correction for the special case of the precharged half-buffer.

Although the results were initially disappointing, as it was formerly believed that unmodified QDI asynchronous circuits would be more resistant to single-event upsets than the Situs analysis showed them to be, final results have been very encouraging. The results show that it is possible to build asynchronous hardware that not only detects but also automatically corrects for upsets with very little speed penalty. In combination with the fact that QDI asynchronous circuits are by their nature tolerant of slow parameter shifts and timing variations, this suggests that it is possible to build high-performance asynchronous hardware that is tolerant to a variety of kinds of noise.

The effort expended so far can be summarized as follows.

1. Different irradiation techniques and test facilities have been investigated. Several large-scale testing facilities have been identified, but the cost and difficulty of using these facilities is high, and on-site alternatives are being investigated.
2. The study of the basic asynchronous building blocks' response to noise modelled as a single bit flip has been initiated with interesting and somewhat unexpected preliminary results.
3. A low-level logic simulator based on the Production Rule model has been designed to simulate the propagation of a single bit flip through a complete asynchronous pipeline. Electrical SPICE simulations have been set up to refine our understanding of the effect of noise on asynchronous operators.
4. Circuit techniques for forcing an SEU to cause a deadlock have been proposed and investigated.
5. System-level techniques for detecting and correcting upsets have been proposed and investigated.
6. Circuit-level techniques for detecting SEUs and also making them self-correcting have been proposed and investigated.

No major problem or deficiency has been encountered, except for regulations restricting the access to radioactive material needed for the radiation hardness tests. The project is slightly behind schedule.

2. Narrative

2.1. Overview

Complementary silicon MOS systems are the most widely used microelectronic systems today. CMOS systems have significant cost, integration, and energy advantages over all other existing fabrication technologies. CMOS systems are vulnerable to radiation damage through a few main effects: transistor-parameter variation due to accumulated charge in the insulating oxide (mainly threshold-voltage shift), single-event upset (SEU) due to photoelectric currents, latchup, and dose-rate effects such as power-supply collapse.

The radiation effect that has received the most attention over the years is the gradual accumulation of radiation damage in the insulating silicon dioxide. The main way this shows up in the circuits is as a gradual shift of the threshold voltage.

There is increasing concern in the semiconductor industry that the shrinking electronic circuits made possible by MOS technology are becoming more sensitive to various kinds of noise upset that have not been adequately studied. Radiation-induced upsets in logic circuits is one kind of such "new" upset, but there is also concern that RF interference is a growing problem, and there is concern that the shrinking feature sizes are making various kinds of self-induced noise more difficult to deal with.

Asynchronous techniques are attractive because they permit circuits to be designed with very few delay assumptions. Quasi delay-insensitive (QDI) design techniques are especially interesting because of the near-total lack of delay assumptions. Such circuits could continue working as designed even when transistor parameters have changed dramatically owing to radiation effects. However, if the threshold voltage shifts too much, even QDI circuits may not work properly—if the threshold voltage becomes negative, so that transistors are turned on all the time, whether their gates are driven or not. To combat this effect, it is possible to add active substrate biasing that would keep the threshold voltage positive. Since it is difficult to know *a priori* what effects the complex interactions of radiation damage and biased substrate on device parameters, QDI circuits would have a real advantage.

As device scaling continues to smaller and smaller feature sizes, the energy levels present in digital CMOS systems will become smaller, and it is expected that digital CMOS systems will become increasingly sensitive to environmental noise. Such increased sensitivity has been observed in an in-

permits the system to correct a few random errors in the memories and if necessary inform the proper diagnostic units of the errors. Errors occurring in latches (or even in the combinational logic between latches) have not been so widely studied and the solutions are less certain. These errors are difficult to detect and correct because designers normally assume that the entire set of state bits in a digital system is correct at all times. The state bits are not correlated in space or meaning in as convenient a way as they are in a RAM, so it becomes very difficult to add extra bits to guard the data. Nevertheless, several techniques have been developed over the years to deal with errors in the logic. Kohavi's *quadded logic*, for instance, permits any bit anywhere in a digital system to be flipped while guaranteeing proper operation. Kohavi's system unfortunately takes four times the hardware of traditional techniques and it is only applicable to relatively low-performance combinational logic. Traditional fault-tolerance techniques such as voting have also been used: build two complete microprocessors and make sure that they store the same values to the memory; if there are any discrepancies, reset the system and try again.

Many techniques for handling SEUs rely on the fact that in many applications, it is sufficient for the system to *detect* that a SEU has occurred; for instance, in real-time control applications it might be acceptable to reset the controller, but it would of course be completely unacceptable to attempt to continue if the data is known to be corrupted. In such systems, QDI asynchronous systems have advantages that clocked systems do not have. The "self-testing" nature of asynchronous systems is well known: stuck-at faults are to a large extent (although not exhaustively) tested by the normal operation of the system—the system deadlocks in most cases that a stuck-at fault is present. Similarly, a SEU would cause deadlock in many cases in a QDI system. The self-testability of a QDI asynchronous system can be enhanced by adding relatively small amounts of extra circuitry, and it is also possible to add extra circuitry to make the detecting of SEUs more probable.

For instance, QDI systems generally use *dual-rail* representation of data: each bit is represented by two circuit nodes, and a "1" is signified by one of those wires' being high, a "0" by the other's being high. One specific type of error that a SEU can cause in a QDI system is that it can cause both data rails to be active simultaneously in a dual-rail channel. This is an illegal state that the circuit is never supposed to enter; adding a small amount of extra circuitry to check for this state would make it possible to detect an appreciable fraction of SEUs in the logic of a QDI system (many other types

of SEU would simply cause deadlock). This circuitry is especially easy to add because the illegal state tends to spread across a QDI system. Therefore, the circuitry would not have to be added everywhere in the system but only at a few well-chosen locations.

The performance gap between hardened and non-hardened technologies is so large that it is worthwhile to investigate circuit-design techniques that trade off even large amounts of speed, energy-efficiency, or area for improved radiation hardness. Theoretical considerations suggest that because of the much thinner gate oxide in modern deep-submicron processes, these new processes should be intrinsically harder than older processes. These results are promising, but there are question marks for more modern technologies; for instance, the most modern deep-submicron technologies do not permit bent transistors, which means that "edgeless" (annular) transistors may not be possible. If standard-edged transistors must be used instead, that means that large leakage currents may bypass the transistor channel under the field oxide.

2.3. Ionizing Radiation Sources

An investigation of suitable facilities for testing of existing asynchronous hardware has been performed. Several testing facilities specializing in validating radiation-hardened chips have been identified. Long-term dose effects can be tested in the vicinity of Situs's facilities in Pasadena (at the California Institute of Technology and at the Jet Propulsion Laboratory). Single-event upsets can be tested at Brookhaven National Laboratory and at Lawrence Berkeley Laboratory. The main interest in this project is, however, to study SEUs that result from ionizing radiation only as an example of a wider class of noise events. Therefore, the exact type of radiation is less important, and the logistical difficulties involved in preparing experiments for use in vacuum chambers and also the extensive travel that would be involved for the Brookhaven and Berkeley facilities makes it attractive to pursue other kinds of sources. Portable radioactive sources that could be used in air would be ideal if they are energetic enough to cause SEU. Polonium-210 alpha irradiators have been tested with disappointing results, and it is not clear that these generate particles with enough energy to cause SEU even in current deep-submicron technologies. Californium-252 is an isotope that has been shown to be useful for SEU studies; it undergoes spontaneous fission, and produces fragments that are much more likely to cause SEUs than the alpha particles of polonium-210 and other common radioactive isotopes. Necessary

radiation safety paperwork has been filed and approved that will permit Situs to proceed with these experiments.

2.4. Change of Focus

Because of comments made to Situs at a DARPA review of the project, the focus of the project has changed somewhat from the proposal. While radiation-induced upsets are still an important part of the project, they are no longer the only focus. Accordingly, Situs has delayed the work on mitigation efforts specific to radiation-induced upsets and has instead concentrated on work that is applicable to noise-induced upsets in general. In other words, Situs has suspended work on methods for mitigating upsets that are dependent on the interaction of radiation and fabrication and/or circuit technologies, and instead the work has been focused on mitigation techniques for soft errors that are assumed to be unavoidable. Techniques that are applicable to errors that "can't be stopped" will likely be applicable to any kind of soft-error source as well as to any kind of fabrication technology (possibly not even restricted to CMOS technology).

2.5. Noise as Single Bit Flip

At the logical level, Situs has studied the effect of noise (radiation or other) when it is modeled as a "single bit flip": a single bit of the logical circuit may flip at any time from zero to one or from one to zero.

A circuit is described at the logical level as a set of *production rules*. Each production rule represents a conditional firing of a node, and in CMOS implementation corresponds to a pull-up or pull-down circuitry. The pair of rules that set and reset a given boolean variable of the circuit (a node) corresponds to what is usually called an operator or gate. There are two types of operators: combinational or state-holding. An operator is combinational when the output node is always connected to either the supply voltage or the ground. It is state-holding otherwise. In a state-holding operator, the value of the output node when it is disconnected from both the voltage supply and the ground is maintained by a pair of cross-coupled inverters called a "staticizer" or "keeper."

In the first digital model considered, it is assumed that a voltage change caused by noise will be corrected when the node on which it occurs is connected to the high voltage supply or the ground by a path of "strong" transistors. The analysis is therefore restricted to the effect of a single bit flip on output nodes of state-holding elements.

The first step of this analysis was to completely characterize the effects of such a fault on the basic pipeline stage called precharged half-buffer (PCHB). The PCHB combines control and datapath and can compute any function on a limited number of input variables; it is the basic building block of the asynchronous systems designed with the Situs toolchain. The result of this analysis shows that single bit flips can lead to three types of errors: (1) the wrong output is produced, (2) an output is lost, (3) an output is duplicated. This result is to some extent a refutation of our initial assumption that a single flip bit would lead to either detectably erroneous data or deadlock (an output's being lost or duplicated *may* lead to deadlock, but also may not, depending on the system design), and makes error recovery a little more complex.

2.6. Error Detection in Asynchronous Datapaths

In absence of a clock reference to indicate when a value on the data wires is valid, the validity has to be coded with the data. Delay-insensitive (DI) codes, which are used in Situs's style of asynchronous logic, are characterized by the following properties. (1) The code has one neutral value distinct from all valid values (the neutral value is usually all zeros). (2) A four-phase handshake protocol takes a data word from the neutral value to a valid value and back to the neutral value. (3) The transitions from neutral to valid and from valid to neutral can be performed by changing the appropriate bits once in any order. (4) A value that is neither neutral nor valid is intermediate: A DI code has to be chosen such that all intermediate values are distinct from the valid values and from the neutral value.

Because of (4), a single bit flip on a valid value leads to a non-valid value (intermediate, neutral, or unused) and can be detected as a fault. However, if the valid value is represented by a single one which is transformed in the all-zero neutral value, the single bit flip may lead to a deadlock. (It might be advantageous to code the data words such that any valid value has at least two ones: in such a case a single bit flip on a valid value always leads to a detectable intermediate or unused value.)

2.7. Development of SEU-tolerant Asynchronous Circuits

A modification to the basic QDI asynchronous circuit design techniques is proposed whereby SEUs can be isolated. Two techniques are proposed. One operates at the system level, and one at the circuit level.

The system-level approach to handling of SEU faults in asynchronous systems depends on the property of *slack elasticity*. The asynchronous sys-

tems in question are designed as dataflow graphs where a computation is represented as streams of values traveling on channels. A system is slack elastic if slack (buffering) can be added to any channel without changing the behavior of the system. If a system is slack elastic and deterministic (most are), the computation can be represented entirely by the sequence of values on the channels. This means that a computation can be verified by running it twice (in space or in time) and comparing the results of the two runs. Situs proposes to perform the necessary comparisons at the chip boundaries. The area overhead of such an approach is 100% compared to a non-SEU-hardened implementation, and calculations made by Situs show that the performance overhead is usually negligible.

The circuit-level approach to handling of SEU faults is based on the properties of *stability* and *noninterference* of quasi delay-insensitive production-rule sets. The approach here is to add extra transistors in order to force a deadlock (which can be detected at the system level) or further extra transistors to force a recovery in case of a single-event upset. The overhead for these solutions is larger than for the system-level solutions, but they are applicable to a wider class of asynchronous systems, and in the case of the self-recovering circuits, are also more powerful than the system-level solution.

Because of the promise shown by the circuit-level techniques for SEU mitigation, and because of the comments made by the program manager at one of the Situs presentations, Situs made the work on circuit-level SEU-mitigation techniques the main focus of the second half of Phase I.

2.8. SEU-detecting Asynchronous Circuits

The first technique being developed at Situs for circuit-level SEU mitigation involves doubling the number of circuit nodes and quadrupling the size of the circuits to force a deadlock. In essence, the technique is based on using a simple repetition code on all logic nodes. A logic "zero" is represented by "zero-zero," and a logic "one" is represented by "one-one" in this code. Any other value, such as "one-zero" or "zero-one" is either a transient phenomenon during normal circuit operation (we cannot assume that the circuit switches instantaneously from "zero-zero" to "one-one"), or it is the result of a SEU. By replacing each literal in each production rule with the conjunction of the new "double" literals, the circuit will wait until the value has stabilized in either the "zero-zero" or "one-one" state. As a circuit that has suffered a SEU will never reach the "zero-zero" or "one-one" state, the result of a SEU will be a system deadlock, which can be detected and

resolved at the system level.

The drawback of the SEU-detecting circuit technique mentioned here is that it increases the size of the circuits. All circuit nodes are doubled, but more importantly, all circuit operators are *also* doubled, both in their complexity and count. Furthermore, all operators become state-holding. Preliminary work has been undertaken to mitigate these effects, and results of this preliminary work are encouraging, as will be described below. It appears likely that many optimizations remain to be discovered, however, and this is especially so in light of the redundancy already built into the QDI circuits (as described in section above). Situs expects that the search for further circuit optimizations will be a significant focus of future work on noise-tolerant asynchronous nanoelectronics.

2.9. SEU-tolerant Asynchronous Circuits

A possibility that has been studied by Situs during Phase I of the project is that of adding local deadlock detection *at the circuit level* to the doubled QDI asynchronous circuits. Because of the property of *stability* that all QDI circuits are endowed with, input events to a circuit element are always left pending until their corresponding output events have occurred. This means that if an SEU were to upset the circuit into not producing the output event, the input events would still be pending, and if the circuit could detect the occurrence of the SEU locally, it would be possible for the still-pending inputs to produce the desired output anew. In such a design, the environment would simply never know that there had been a SEU—the SEU would be locally self-correcting.

Initial work on SEU-tolerant asynchronous circuits has shown promising results. The proposed circuit style is an enhancement of the simple deadlocking doubled technique mentioned above. At the present time, indications are that with somewhat more overhead than for the deadlocking doubled technique, the circuits can be made entirely SEU-tolerant. Situs intends to continue work on the SEU-tolerant family in the future, at which time the design procedure for these circuits will be finalized.

2.10. Doubled Precharged Half Buffer

Research at Caltech and elsewhere has shown that a circuit structure known as a “precharged half-buffer” (PCHB) is a powerful enough building block that it can be used to construct a large variety of digital circuits. Caltech’s MiniMIPS processor, a clone of the MIPS R3000 microprocessor, consists largely of PCHBs, and the current Caltech project, the Lutonium 8051

microcontroller, makes even more use of PCHBs.

Given the prevalence of PCHBs in recent successful asynchronous design projects, Situs has investigated the consequences of adding SEU-hardening or SEU-tolerance to PCHBs in particular (as opposed to adding the features to an arbitrary asynchronous circuit). Results gathered during Phase I of the project show that it is possible to optimize the SEU-hardened circuits in the particular case of the deadlocking doubled PCHB and in the case of the non-deadlocking doubled PCHB. Designs currently under development at Situs indicate that the circuit complexity referred to in section can be largely, although not entirely, avoided for the PCHB. The proposed *DPCHB* (doubled PCHB) is between two and four times the area of a standard PCHB, but the performance figures are nearly as good: the throughput is 20–30% lower, and most importantly, the forward latency is similar.

The DPCHB work has shown very encouraging results. The conclusion is that by paying a price in energy and area, it is possible to build noise-tolerant asynchronous circuits with very little speed penalty.

2.11. Contract Delivery Status

The contract is completed.

2.12. Report Preparers

The report was prepared by Alain J. Martin, PI, and Mika Nyström.